CLAIMS

What is claimed is:

1. A method of forming an interconnect line in an integrated circuit, the method comprising:

depositing a sacrificial layer overlying a metallization level;

forming an opening in the sacrificial layer;

depositing a metal in the opening, the metal being coupled to an interconnect line in the metallization level; and

etching the sacrificial layer using a chemistry that includes a noble gas fluoride to create an air core overlying the metallization level.

2. The method of claim 1 further comprising the act of planarizing the metal prior to exposing the sacrificial layer.

3. The method of claim 1 further comprising the act of depositing a topside layer overlying the air core.

4. The method of claim 1 further comprising the act of depositing a capping layer overlying the sacrificial layer prior to forming an opening in the sacrificial layer.

5. The method of claim 1 wherein the sacrificial layer is deposited overlying a support layer.

6. The method of claim 1 wherein the opening includes a via.

7. The method of claim 1 wherein the metal includes copper.

8. The method of claim 1 wherein the noble gas fluoride includes xenon difluoride.

9. The method of claim 1 wherein the sacrificial layer includes polycrystalline silicon.

10. The method of claim 4 wherein the capping layer includes silicon nitride.

11. The method of claim 1 wherein the metallization level includes a damascene structure.

12. In an integrated circuit, a structure comprising:

a first interconnect line;

a via underlying the interconnect line;

a second interconnect line underlying the via, the second interconnect line being coupled to the first interconnect line through the via; and

an air core between the first interconnect line and the second interconnect line.

13. The structure of claim 12 wherein the first interconnect line and the via form a damascene structure.

14. The structure of claim 12 wherein the first interconnect line is of a material that includes copper.

15. The structure of claim 12 further comprising a top side layer overlying the first interconnect line.

16. The structure of claim 12 wherein a portion of the via is in a support layer.

17. The structure of claim 12 further comprising a capping layer between the support layer and the second interconnect line.

18. A damascene structure comprising:

means for electrically coupling a first level interconnect line to a second level interconnect line;

means for structurally supporting the second level interconnect line; and

means for providing a unity-k dielectric region between the first level interconnect line and the second level interconnect line.

19. The structure of claim 18 wherein the means for providing a unity-k dielectric region includes an air core.

20. The structure of claim 18 wherein the means for structurally supporting the second level interconnect line includes a layer that includes silicon dioxide.